What is claimed is:

~~Claims~~

1. A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer ~~(4; 24)~~, which is applied to a first main surface of a first semiconductor wafer ~~(2; 26)~~, so as to produce a recess ~~(6; 20, 22, 30)~~;

b) connecting the first semiconductor wafer ~~(2; 26)~~ via the first intermediate layer ~~(4; 24)~~ to a second semiconductor wafer ~~(8; 28)~~ in such a way that a hermetically sealed cavity ~~(12; 20, 22, 30)~~ is defined by the recess;

c) thinning one of the wafers ~~(2; 26)~~ from a surface facing away from said first intermediate layer ~~(4; 24)~~ so as to produce a diaphragm-like structure ~~(14; 32, 36)~~ on top of the cavity ~~(12; 20, 22)~~;

d) producing electronic components ~~(16)~~ in said thinned semiconductor wafer ~~(2; 26)~~;

e) providing at least one further intermediate layer between the two semiconductor wafers, which, prior to the connection of the two semiconductor wafers, is structured, in such a way that the structure formed in said at least one further intermediate layer and the recess in said first intermediate layer define the cavity; and

fe) producing at least one defined opening ~~(36)~~ so as to provide access to the hermetically sealed cavity ~~(20, 22)~~.

2. A method according to claim 1, wherein the main surface of the second semiconductor wafer ~~(8)~~, which is connected to the first semiconductor wafer ~~(2)~~ via the intermediate layer ~~(4)~~, has applied thereto a second intermediate layer ~~(10)~~ prior to the connecting step.

3. A method according to claim 2, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

4. A method according to ~~one of the~~ claims ~~1 to 3~~, wherein~~,~~ ~~in addition to the first intermediate layer, further intermediate layers are provided between the two semiconductor wafers, said intermediate layers being structured before the two semiconductor wafers are connected, so as to produce~~ a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

5. A method according to ~~one of the~~ claims ~~1 to 4~~, wherein the first and the second wafer ~~(2, 8; 26, 28)~~ consist of silicon.

6. A method according to ~~one of the~~ claims ~~1 to 5~~, wherein said ~~one or said~~ plurality of intermediate layers consist~~(s)~~ of an oxide, a polysilicon, a nitride or of metal.

7. A method according to ~~one of the~~ claims ~~1 to 6~~, wherein said ~~one or said plurality of~~ intermediate layers ~~(24)~~ are structured in such a way that, after the connection of the two wafers ~~(26, 28)~~, a plurality of cavities ~~(20, 22)~~ is defined, said cavities being interconnected by channels ~~(30)~~ and hermetically sealed from their surroundings.

8. A method according to ~~one of the~~ claims ~~1 to 7~~, wherein the connection in step b) is carried out in a vacuum.

9. A method according to ~~one of the~~ claims ~~1 to 11~~, wherein an SOI wafer is used as a first ~~(2; 26)~~ and/or second ~~(8; 28)~~ wafer.

10. A method according to ~~one of the~~ claims ~~1 to 9~~, wherein said at least one defined opening ~~(36)~~ is produced in the diaphragm-like structure ~~(34)~~.

11. A method according to claim 10, wherein said at least one defined opening ~~(36)~~ is produced in the diaphragm-like structure ~~(34)~~ by means of a needle, a blade, by the use of a pulsed laser radiation or by etching.

~~12. A method according to one of the claims 1 to 9, wherein a plurality of micro-electromechanical structures is produced in a wafer, said method comprising in addition the step of dicing the individual micromechanical structures so as to obtain chips, said at least one defined opening, which provides access to the hermetically sealed cavity, being produced by the dicing step.~~

~~13. A method according to one of the claims 1 to 12, wherein said one or said plurality of intermediate layers (24) is/are structured in step a) in such a way that, after the connection of the two wafers (26, 28), at least two hermetically sealed cavities (20, 22) interconnected by a channel (30) are defined, a diaphragm-like structure (32, 34) being arranged on top of each of said cavities (20, 22) after step c), and a defined opening (36) through said diaphragm-like structure (34) of one of the cavities (22) being produced in step c).~~

~~14~~12. A method according to claim ~~13~~7, wherein the channel is structured in the fashion of a labyrinth in step a) in such a way that disturbing products formed during the production of the opening are prevented from passing said channel.

~~15. A method according to one of the claims 1 to 12, wherein a plurality of defined openings is produced in the diaphragm-like structure in step c) in such a way that, after the production of the openings, the diaphragm-like structure forms a supporting structure for the movable mass of an acceleration sensor.~~

13. A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, so as to produce a recess;

b) connecting the first semiconductor wafer via the first intermediate layer to a second semiconductor

wafer in such a way that a hermetically sealed cavity is defined by the recess;

c) thinning one of the wafers from a surface facing away from said first intermediate layer so as to produce a diaphragm-like structure on top of the cavity;

d) producing electronic components in said thinned semiconductor wafer; and

e) dicing a plurality of micro-electromechanical structures, which are formed in a wafer according to steps a) to d), so as to obtain chips, a defined opening, which provides access to the hermetically sealed cavities, being produced by the dicing step.

14. A method according to claim 13, wherein the main surface of the second semiconductor wafer, which is connected to the first semiconductor wafer via the intermediate layer, has applied thereto a second intermediate layer prior to the connecting step.

15. A method according to claim 14, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

16. A method according to claim 13, wherein a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

17. A method according to claim 13, wherein the first and the second wafer consist of silicon.

18. A method according to claim 13, wherein said intermediate layer consist of an oxide, a polysilicon, a nitride or of metal.

19. A method according to claim 13, wherein said intermediate layers are structured in such a way that, after the connection of the two wafers, a plurality of cavities is defined, said cavities being interconnected by channels and hermetically sealed from their surroundings.

20. A method according to claim 13, wherein the connection in step b) is carried out in a vacuum.

21. A method according to claim 13, wherein an SOI wafer is used as a first and/or second wafer.

22. A method according to claim 19, wherein the channel is structured in the fashion of a labyrinth in step a) in such a way that disturbing products formed during the production of the opening are prevented from passing said channel.

23. A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, so as to produce a recess;

b) connecting the first semiconductor wafer via the first intermediate layer to a second semiconductor wafer in such a way that a hermetically sealed cavity is defined by the recess;

c) thinning one of the wafers from a surface facing away from said first intermediate layer so as to produce a diaphragm-like structure on top of the cavity;

d) producing electronic components in said thinned semiconductor wafer;

wherein in step a) the intermediate layer is structured in such a way that, when the two wafers have been connected, at least two hermetically sealed cavities are defined, which are interconnected by a channel, a respective diaphragm-like structure being arranged on top of each of said cavities after step c),

and wherein the method additionally comprises the step e) of opening a defined opening through the diaphragm-like structure on top of one of the cavities.

24. A method according to claim 23, wherein the main surface of the second semiconductor wafer, which is connected to the first semiconductor wafer via the intermediate layer, has applied thereto a second intermediate layer prior to the connecting step.

25. A method according to claim 24, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

26. A method according to claim 23, wherein a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

27. A method according to claim 23, wherein the first and the second wafer consist of silicon.

28. A method according to claim 23, wherein said intermediate layer consists of an oxide, a polysilicon, a nitride or of metal.

29. A method according to claim 23, wherein the connection in step b) is carried out in a vacuum.

30. A method according to claim 23, wherein an SOI wafer is used as a first and/or second wafer.

31. A method according to claim 23, wherein said at least one defined opening is produced in the diaphragm-like structure by means of a needle, a blade, by the use of a pulsed laser radiation or by etching.

32. A method according to claim 23, wherein the channel is structured in the fashion of a labyrinth in step a) in such a way that disturbing products formed during the production of the opening are prevented from passing said channel.

33. A method of producing a micro-electromechanical element comprising the following steps:

a) structuring a first intermediate layer, which is applied to a first main surface of a first semiconductor wafer, so as to produce a recess;

b) connecting the first semiconductor wafer via the first intermediate layer to a second semiconductor wafer in such a way that a hermetically sealed cavity is defined by the recess;

c) thinning one of the wafers from a surface facing away from said first intermediate layer so as to produce a diaphragm-like structure on top of the cavity;

d) producing electronic components in said thinned semiconductor wafer; and

e) producing a plurality of defined openings in the diaphragm-like structure in such a way that, when said openings have been produced, the diaphragm-like structure forms a supporting structure for the movable mass of an acceleration sensor.

34. A method according to claim 33, wherein the main surface of the second semiconductor wafer, which is connected to the first semiconductor wafer via the intermediate layer, has applied thereto a second intermediate layer prior to the connecting step.

35. A method according to claim 34, wherein the second intermediate layer is structured in such a way that, after the connecting step, the structure formed in the second intermediate layer and the recess in the first intermediate layer define the cavity.

36. A method according to claim 33, wherein a cavity with areas of variable height is produced due to the use of a plurality of intermediate layers.

37. A method according to claim 33, wherein the first and the second wafer consist of silicon.

38. A method according to claim 33, wherein said intermediate layer consists of an oxide, a polysilicon, a nitride or of metal.

39. A method according to claim 33, wherein the connection in step b) is carried out in a vacuum.

40. A method according to claim 33, wherein an SOI wafer is used as a first and/or second wafer.

41. A method according to claim 33, wherein said openings are produced in the diaphragm-like structure by means of a needle, a blade, by the use of a pulsed laser radiation or by etching.